

# **JMV4852P**

**Product Preview** 

**30V 32A P-Channel MOSFET** 



#### **Features**

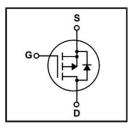
- Advanced trench technology
- Ultra-low on-resistance
- RoHS compliant
- 100% avalanche tested

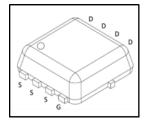


Product Summary				
V <sub>DS</sub>	-30V			
	7.6 mΩ (Typ.)			
R <sub>DS(ON)</sub>	9.8 mΩ (Max.)			
I <sub>D</sub>	-32A			

## **Applications**

- Motor controllers
- DC-to-DC convertors
- Battery-driven electronic products, electrical equipment and machines





### **Ordering Information**

Part Number	Marking	Package	Packaging
JMV4852P	V4852P	DFN3.3x3.3	Tape & Reel



## **Absolute Maximum Ratings**

Parameter	Symbol	Limit	Unit
Drain-to-Source Voltage	V <sub>DS</sub>	-30	.,
Gate-to-Source Voltage	$V_{GS}$	±20	V
Continuous Drain Current, Package Limited (T <sub>C</sub> = 25°C) (1)	I <sub>D</sub>	-32	
Continuous Drain Current, Silicon Limited (T <sub>C</sub> = 25°C) (1)	I <sub>D</sub>	-58	
Continuous Drain Current, Silicon Limited (T <sub>C</sub> = 100°C) (1)	I <sub>D</sub>	-36	_
Continuous Drain Current, Silicon Limited t (T <sub>A</sub> = 25°C) (2), (5)	I <sub>D</sub>	-11	A
Continuous Drain Current , Silicon Limited (T <sub>A</sub> = 100°C) (2), (5)			
Pulsed Drain Current (3)	I <sub>DM</sub>	-128	
Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>D</sub>	52.1	W
Linear Derating Factor	-	0.42	W/°C
Single Pulse Avalanche Energy (4)	E <sub>AS</sub>	75	mJ
Avalanche Current	I <sub>AS</sub>	28	Α
Junction Temperature	T <sub>J</sub>	-55 to 150	0.0
Storage Temperature	T <sub>STG</sub>	-55 to 150	°C

### **Thermal Characteristics**

Parameter	Symbol	Max	Unit
Junction-to-Ambient Thermal Resistance (5)	$R_{\theta JA}$	62	°C/M
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	2.4	°C/W

# Static Electrical Characteristics (6)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Drain-to-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	٧
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$ , $I_{D} = -250 \mu A$	-1.0	-	-2.0	V
Drain-to-Source Leakage Current	I <sub>DSS</sub>	$V_{DS} = -30V, V_{GS} = 0V$	-	-	-1	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	±100	nA
Drain to Source On Bosistance	D	V <sub>GS</sub> = -10V, I <sub>D</sub> = -10A	-	7.6	9.8	mΩ
Drain-to-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -10A	-	9.5	12.3	mΩ



# Dynamic Electrical Characteristics (6)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Forward Transconductance	<b>g</b> fs	V <sub>DS</sub> = -5V, I <sub>D</sub> = -20A	-	68	-	S
Total Gate Charge	Qg	V <sub>GS</sub> = -10V,	-	64	-	
Gate-to-Source Charge	$Q_{gs}$	V <sub>DS</sub> = -15V,	-	9	-	nC
Gate-to-Drain Charge	$Q_{gd}$	I <sub>D</sub> = -20A	-	10	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = -10V,	-	6	-	
Rise Time	t <sub>r</sub>	V <sub>DS</sub> = -15V,	-	22	-	
Turn-Off Delay Time	t <sub>d(off)</sub>	I <sub>D</sub> = -20A,	-	84	-	ns
Fall Time	t <sub>f</sub>	$R_G = 3.0\Omega$	-	17	-	
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V,	-	2950	-	
Output Capacitance	C <sub>oss</sub>	f = 1MHz,	-	275	-	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	V <sub>DS</sub> = -15V	-	130	-	

# **Diode Characteristics** (6)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_S = -10A$	-	-0.9	-	V
Reverse Recovery Time	t <sub>rr</sub>	$V_{GS} = 0V$ , $I_S = -10A$ ,	-	40	-	ns
Reverse Recovery Charge	Q <sub>rr</sub>	$dI_s/dt = -100A/\mu s$	-	43	-	nC

- (1) Rated according to  $R_{\theta \text{JC}}.$
- (2) Rated according to  $R_{\theta JA}. \label{eq:Relation}$
- (3) Limited by maximum  $T_J$ .
- (4)  $T_A = 25$ °C, L = 0.1mH,  $I_{AS} = 28$ A.
- (5) Surface–mounted on 1 inch² FR4 board, 2 oz Cu.
- (6)  $T_J = 25$ °C unless otherwise specified.

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### **Typical Electrical Characteristics**

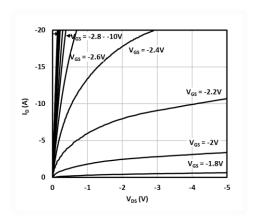


Fig. 1 Output characteristics

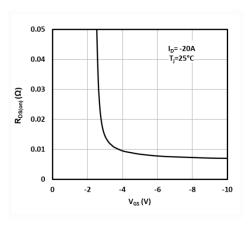


Fig.3 On-resistance vs. gate voltage

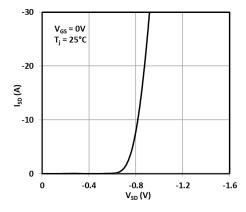


Fig.5 Source-to-drain diode forward characteristics

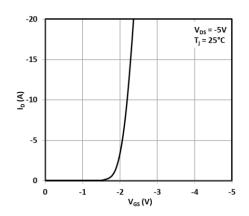


Fig. 2 Transfer characteristics

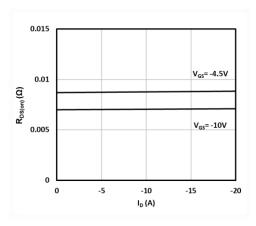


Fig.4 On-resistance vs. drain current

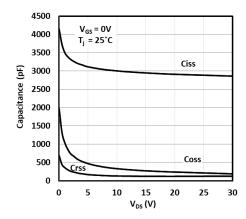


Fig.6 Capacitance vs. drain-to-source voltage



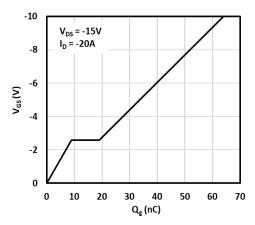


Fig.7 Gate-to-source voltage vs. gate charge

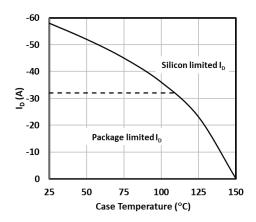


Fig.8 Maximum drain current vs. case temperature

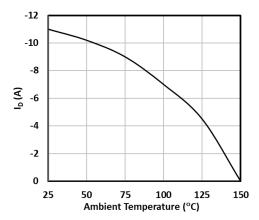
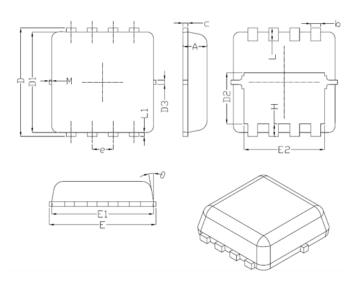


Fig. 9 Maximum drain current vs. ambient temperature

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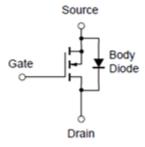
# **Package Drawing**



DIM.	N	1ILLIMETER	rs.
DIIVI.	MIN.	NOM.	MAX.
Α	0.70	0.80	0.90
b	0.25	0.32	0.39
С	0.10	0.15	0.25
D	3.00	3.30	3.60
D1	3.00	3.10	3.50
D2	1.48	2.00	2.20
D3	-	0.20	
Ε	3.00	3.30	3.60
E1	3.00	3.10	3.25
E2	2.29	2.49	2.69
e		0.65 BSC	
Н	0.15	0.25	0.50
L	0.15	0.40	0.60
L1	0.05	0.15	0.25
α	8°	10°	12°
М		0.10	

**DFN 3.3x3.3** 

# **Equivalent Circuit**





### Revision history of JMV4852P specification

Version	Change Items	Effective Date
1.00	Initial Release	28-Feb-20



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